

**Amendments to the Claims:**

A listing of the entire set of pending claims (including amendments to the claims, if any) is submitted herewith per 37 CFR 1.121. This listing of claims will replace all prior versions, and listings, of claims in the application.

**Listing of Claims:**

1. (Currently amended) ~~A multiplier~~ Multiplier device comprising:  
\_\_\_\_\_ first to  $n^{\text{th}}$  multipliers  $M_1$  to  $M_n$  for multiplying that are configured to multiply a  
carrier modulated information signal with first to  $n^{\text{th}}$  mutually phase shifted and  
identical, substantially square wave mixing signals  $MS_1$  to  $MS_n$  with 50% duty cycle,  
wherein  $n$  is greater than 2,  
\_\_\_\_\_ first to  $n^{\text{th}}$  weighting circuits with respective fixed weighting factors  $WF_1$  to  $WF_n$   
that are configured to receive characterized by  $n$  being greater than 2, corresponding  
outputs of said the multipliers  $M_1$  to  $M_n$ , and to produce therefrom corresponding  
weighted outputs being respectively coupled through weighting circuits  $W_1$  to  $W_n$  with  
respective fixed weighting factors  $WF_1$  to  $WF_n$  to  
\_\_\_\_\_ an adder circuit that is configured to provide a sum of the weighted outputs,  
wherein:  
\_\_\_\_\_ the said mixing signals  $MS_1$  to  $MS_n$  having have respective phase angles  $\phi_i$   
corresponding to  $\phi_i = i * \Delta\phi$ , and  
\_\_\_\_\_ the said weighting factors  $WF_i$  corresponding to the sine values of said  
respective phase angles  $\phi_i = i * \Delta\phi$ , with  $\Delta\phi$  being the mutual phase difference  
between each two phase consecutive mixing signals corresponding to  $\pi/(n + 1)$  and  $i$   
varying from 1 to  $n$ .
  
2. (Currently amended) ~~Multiplier~~ The multiplier device according to of claim 1,  
characterized by wherein  $n$  corresponding corresponds to  $(N+1)/2$  for an elimination  
of all harmonics up to the  $N^{\text{th}}$  order from the an output of said the adder circuit.

3. (Currently amended) ~~Multiplier~~ The multiplier device according to of claim 1 or 2,  
~~characterized by said wherein the~~ mixing signals  $MS_1$  to  $MS_n$  ~~being are~~ derived from  
 a local oscillator signal with frequency  $f_0$  ~~through an arrangement of fixed phase shift~~  
~~means and/or frequency divider means.~~

4. (Currently amended) ~~Multiplier~~ The multiplier device according to of claim 3,  
~~characterized by including:~~  
\_\_\_\_\_ a local oscillator circuit, and supplying an oscillator signal with frequency  $f_0$  to  
\_\_\_\_\_ a serial arrangement of first to  $n^{\text{th}}$  phase shifting means shifters that is  
configured to receive an oscillator signal with frequency  $f_0$  from the local oscillator  
circuit, each phase shifter providing a fixed phase shift of  $\Delta\phi$  and supplying  
respectively mixing signals  $MS_1$  to  $MS_n$  to said the first to  $n^{\text{th}}$  multipliers  $M_1$  to  $M_n$ .

5. (Currently amended) ~~Multiplier~~ The multiplier device according to of claim 4,  
~~characterized by said wherein the~~ local oscillator circuit ~~generating includes:~~  
\_\_\_\_\_ an oscillator that is configured to provide a clock control signal with clock  
frequency  $n * f_0$ , being supplied through  
\_\_\_\_\_ a frequency divider with dividing factor  $n$  that is configured to receive the clock  
control signal and to provide a frequency divided output signal to said the serial  
arrangement of first to  $n^{\text{th}}$  phase shifting means shifters, each phase shifter of said  
first to  $n^{\text{th}}$  phase shifting means comprising including a D-flip-flop being that is clock  
controlled by said the clock control signal and providing said to provide the fixed  
phase shift of  $\Delta\phi$ .

6. (New) The multiplier device of claim 3, including  
 a plurality of fixed phase shift devices that are configured to receive the local  
 oscillator signal and provide therefrom the mixing signals.

7. (New) The multiplier device of claim 3, including  
 a plurality of frequency dividers that are configured to receive the local  
 oscillator signal and provide therefrom the mixing signals.

8. (New) The multiplier device of claim 2, wherein the mixing signals  $MS_1$  to  $MS_n$  are derived from a local oscillator signal with frequency  $f_0$ .

9. (New) The multiplier device of claim 8, including  
a plurality of fixed phase shift devices that are configured to receive the local oscillator signal and provide therefrom the mixing signals.

10. (New) The multiplier device of claim 10, including  
a plurality of frequency dividers that are configured to receive the local oscillator signal and provide therefrom the mixing signals.

11. (New) The multiplier device of claim 8, including  
a local oscillator circuit, and  
a serial arrangement of first to  $n^{\text{th}}$  phase shifters that is configured to receive an oscillator signal with frequency  $f_0$  from the local oscillator circuit, each phase shifter providing a fixed phase shift of  $\Delta\phi$  and supplying respectively mixing signals  $MS_1$  to  $MS_n$  to the first to  $n^{\text{th}}$  multipliers  $M_1$  to  $M_n$ .

12. (New) The multiplier device of claim 11, wherein the local oscillator circuit includes:

an oscillator that is configured to provide a clock control signal with clock frequency  $n * f_0$ , and

a frequency divider with dividing factor  $n$  that is configured to receive the clock control signal and to provide a frequency divided output signal to the serial arrangement of first to  $n^{\text{th}}$  phase shifters, each phase shifter including a D-flip-flop that is clock controlled by the clock control signal to provide the fixed phase shift of  $\Delta\phi$ .